

CLAIMS

What is claimed is:

1. A device comprising a drain, a gate, and a source wherein the device acts like a NMOS when drain to source (VDS) and gate to source (VGS) voltages are positive, and acts like a PMOS when drain to source (VDS) and gate to source (VGS) voltages are negative.
2. The device of claim 1 wherein the device is a metal insulator semiconductor field effect transistor (MISFET) comprising source, drain, and gate regions wherein the electrostatic potential in each of the source, drain, and gate regions is symmetric for electrons and holes, with the source to channel interface being different from the channel to drain interface.
3. The MISFET of claim 2 wherein the source to channel barrier height can be modulated by a field-effect, and the channel to drain barrier height is not affected by gate bias.
4. The MISFET of claim 2 comprising:
 - a source layer being made with a material having a source band-gap (EG2) and a source mid-gap value (EGM2), said source layer having a source Fermi-Level (EF2);
 - a drain layer having a drain Fermi-Level (EF4);
 - a channel layer between the source layer and the drain layer, said channel layer being made with a material having a channel band-gap (EG3) and a channel mid-gap value (EGM3), said channel layer having a channel Fermi-Level (EF3);
 - a source contact layer connected to the source layer opposite the channel layer, said source contact layer having a source contact Fermi-Level (EF1); and
 - a gate electrode having a gate electrode Fermi-Level (EF6)wherein:
 - said source band-gap (EG2) is substantially narrower than said channel band-gap (EG3);
 - said source contact Fermi-Level (EF1), said source Fermi-Level (EF2), said channel Fermi-Level (EF3), said drain Fermi-Level (EF4) and said gate electrode Fermi-Level (EF6) are equal to said source mid-gap value (EGM2) and said channel

mid-gap value (EGM3), within a predetermined tolerance value, when no voltage is applied to the device.

5. The MISFET of claim 4, wherein the first band-gap is at least 9 to 10 times narrower than said second band-gap.
6. The MISFET of claim 5, wherein the first band-gap (EG2) is in the order of 0.1 to 0.12 electron-volts (eV) and the second band-gap (EG3) is in the order of 1.0 to 1.2 electron-volts (eV).
7. The MISFET of any one of the preceding claims, wherein the predetermined tolerance value is lower than 10%, respectively, preferably lower than 5% of the channel band-gap.
8. The MISFET of claim 4 comprising:
 - a epitaxial titanium nitride (TiN) source contact;
 - a source layer coupled to the source contact, the source layer comprising $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ alloys, or superlattices of alternating $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-y}\text{C}_y$;
 - an un-doped silicon (Si) channel layer coupled to the source layer;
 - an epitaxial titanium nitride (TiN) drain layer coupled to the channel layer;
 - a titanium nitride (TiN) gate electrode coupled to at least one of the source layer, channel layer, and drain layer via an insulator.
9. The MISFET of claim 1 comprising a channel, the channel consisting essentially of Ge or strained-layer short period superlattices of GeSiSn/Ge , or GeSi/SeSn or SiSn/Ge .
10. The MISFET of claim 1 wherein the source consists essentially of $\text{Ge}_1\text{-Sn}_1$ strained-layer short period superlattices, strained to $\langle 111 \rangle$ Ge substrates.
11. The MISFET of claim 1 wherein the source comprises a material having a band-gap around 0.1eV.
12. The MISFET of claim 1 comprising a source contact that is a conductor whose Fermi-level is aligned with the mid-gap point of the source and channel materials.

13. The MISFET of claim 1 wherein the drain comprises a material that is a conductor whose Fermi-level is aligned with the mid-gap point of the source and channel materials.
15. The MISFET of claim 1 comprising a source contact and a gate electrode wherein the same materials are used for the source contact, drain, and gate electrode.
14. The MISFET of claim 1 comprising a gate electrode, the gate electrode comprising a material that is a conductor whose Fermi-level is aligned with the mid-gap point of the source and channel materials.
15. The MISFET of claim 1 wherein the gate comprises at least one of: GeON (germanium oxynitride), ZrO₂ and, BaTiO.
16. A circuit comprising at least one device having a source terminal, the device alternately behaving as an NMOS device and a PMOS device as the voltage at the source terminal is varied.
17. The circuit of claim 16 wherein the circuit is one of an inverter, a logic gate, and a memory cell.
18. A device comprising a single source, a single drain, and a plurality of gates.
19. A device comprising a drain, a source, gate(s), and source, gate, and drain electrodes, wherein:
the source is coupled to the channel at a source to channel interface;
the channel is coupled to the drain at a channel to drain interface;
the source to channel interface differs from the channel to drain interface; and
the electrostatic potential for electrons and holes is symmetric with respect to the mid-gap level, along a cut from source to drain, on a plane near an interface with a gate and on a plane far from an interface with a gate, when zero voltage is applied to the source, drain, and gate electrodes.
20. A device comprising a drain, a source, and gate(s) wherein:
the source is coupled to the channel at a source to channel interface;
the channel is coupled to the drain at a channel to drain interface;

the source to channel interface differs from the channel to drain interface; and any cut along a line perpendicular to the plane of a gate, through the source layers, or through the channel layers, or the drain layers, exhibits a flat band condition along that line.